ABSTRACT

A fast error diagnosis system and process for combinational verification is described. The system and process localizes error sites in a combinational circuit implementation that has been shown to be inequivalent to its specification. In the typical case, it is not possible to identify the error location exactly. The invention uses a diagnosis strategy of gradually increasing the level of detail in the analysis algorithm to ultimately derive a small list of potential error sites in a short time. The invention combines the use of simulation, Binary Decision Diagrams, and Boolean satisfiability in a novel way to achieve the goal. The previous approaches have been limited in that they have either been constrained to a specific error model unlike the present invention, or they are inefficient in comparison to the present invention. . The present invention allows for the final set of error sites derived to be small, where that set contains the actual error sites, and is derived in a reasonable amount of time.